EE/CPRE/SE 491 - sddec24-13

ReRAM Compute ASIC Fabrication

Weekly Report 6

3/05/24 - 3/19/24

Client: Prof. Henry Duwe

Advisor: Prof. Cheng Wang

Team Members:

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog digital designer
- Nathan Cook – Main client liaison, mixed analog digital designer
- Jason Xie – Assistant documentation editor, main digital designer

Weekly summary:

This week, we solved the issue integrating the inverter into the Caravel harness. We prototyped a comparator for use in our ADC and are working on choosing the process parameters. We also began work on a transimpedance amplifier.

Past Week Accomplishments:

- Began designing the transimpedance amplifier
- Simulated a comparator in xschem
- Researched ReRAM architectures to better understand the behavior and characteristics of it

Individual Contributions:

Team Member	Contributions	Weekly hours	Total Hours
Konnor Kivimagi	Solved caravel harness integration issue. Started organizing for documentation	5	40
Gage Moorman	Began testing Dynamic comparator structure and researched TIA structures.	8	42
Nathan Cook	Researched and recorded ReRAM architectures	7	40
Jason Xie	Began designing transimpedance amplifier. Worked on implementing behavioral ReRam model from previous team.	6	40

Pending Issues:

- ReRAM instances within xschem are not simulating properly
- No straightforward way to analyze xschem/ngspice data on outside applications

Plans for the coming week:

- Gage Moorman
    - Size transistors in comparator design
    - Begin prototyping ADC design
    - Formulate a process using gm/id sizing method for transistors
- Konnor Kivimagi
    - Work on improving our documentation
    - Look into interfacing with ReRAM crossbar
- Nathan Cook
    - Continue working on digital design of components
    - Begin some derivation of projected values required and document them
- Jason Xie
    - Define interface components and assist with digital design of components
    - Determine transimpedance amplifier device parameters

Summary of Advisor Meeting:

This week we discussed the first iteration of our design document and received feedback on what could be improved. We discussed researching the different architectures of ReRAM to find out if there was an optimal orientation of the source line bit line and worldline. We also had another discussion about our users better laid out what their needs would be.